WHAT IS CLAIMED IS:

1. A frequency divider comprising:

a sequence of divide stages coupled to provide a plurality of different divide ratios; and

at least one multiplexer coupled to selectively feed back the output of a first divide stage to an input of a divide stage earlier in the sequence of divide stages.

2. The frequency divider of claim 1 further comprising at least one input coupled to receive a programmable control signal indicating which of the plurality of different divide ratios to apply.

3. The frequency divider of claim 1 further comprising an input to receive a signal to be divided.

4. The frequency divider of claim 3 wherein respective divide stages include clock inputs coupled to the signal to be divided.

5. The frequency divider of claim 1 further comprising

a duty-cycle stage coupled to correct a duty cycle of outputs having an odd divide ratio.

6. The frequency divider of claim 5, wherein the duty-cycle stage includes:

a first input to receive a first signal having an unbalanced duty cycle;

a second input to receive a second signal, wherein the second signal is a delayed version of the first signal; and

logic to generate a signal having a balanced duty cycle using the first signal and the second signal.

7. The frequency divider of claim 1 wherein respective ones of the divide stages include an activation input coupled to receive an activation signal to selectively turn off respective divide stages if the respective divide stages are not used for a selected divide ratio.

8. The frequency divider of claim 1 further including self-correction logic.

9. The frequency divider of claim 8 further including a latch circuit, the latch circuit including:

one or more portions of self-correction logic; and

selection circuitry implementing the at least one multiplexer.

10. The frequency divider of claim 9, wherein:

the selection circuitry is coupled to select respective portions of the self-correction logic based on a selected divide ratio; and wherein

the latch is coupled to outputs of respective portions of the self-correction logic to provide a differential indication of a logic value produced by the selected logic portion.

11. A frequency divider comprising a plurality of divide stages programmably coupled to provide a plurality of different divide ratios.

12. The frequency divider of claim 11 further comprising at least one multiplexer coupled to selectively couple an output of a first divide stage to an input of a second divide stage.

13. The frequency divider of claim 11 further comprising

a duty-cycle stage coupled to correct a duty cycle of outputs having an odd divide ratio.

14. The frequency divider of claim 13, wherein the duty-cycle stage includes:

a first input to receive a first signal having an unbalanced duty cycle;

a second input to receive a second signal, wherein the second signal is a delayed version of the first signal; and

logic to generate a signal having a balanced duty cycle using the first signal and the second signal.

15. The frequency divider of claim 11 wherein respective ones of the divide stages include an activation input coupled to receive an activation signal to selectively

turn off respective divide stages if the respective divide stages are not used for a selected divide ratio.

16. The frequency divider of claim 11 further including self-correction logic.

17. The frequency divider of claim 16 further including a latch circuit, the latch circuit including:

one or more portions of the self-correction logic; and

selection circuitry implementing a multiplexer.

18. The frequency divider of claim 17, wherein:

the selection circuitry is coupled to select respective portions of the self-correction logic based on a selected divide ratio; and wherein

the latch is coupled to outputs of respective portions of the self-correction logic to provide a differential indication of a logic value produced by the selected logic portion.

19. The frequency divider of claim 11, wherein the plurality of divide stages are programmably coupled to produce an output having a divide ratio selected from the following group of divide ratios: 1/11, 1/9, 1/7, 1/6, 1/5, and 1/4.

20. A clock generation circuit comprising:

an input coupled to receive a signal having a first frequency;

an output coupled to provide a clock signal having a frequency derived from the first frequency;

a divider coupled to the input and the output, the divider including:

a sequence of synchronous divide stages to provide a plurality of different divide ratios; and

one or more multiplexers to selectively feed-back an output of a divide stage to an input of a divide stage earlier in the sequence.

21. The clock generation circuit of claim 20 wherein the divider further includes a duty-cycle stage coupled to correct a duty cycle of outputs having an odd divide ratio.

22. The clock generation circuit of claim 21, wherein the duty-cycle stage includes:

a first input to receive a first signal having an unbalanced duty cycle;

a second input to receive a second signal, wherein the second signal is a delayed version of the first signal; and

logic to generate a third signal having a balanced duty cycle using the first signal and the second signal.

23. The clock generation circuit of claim 20 wherein respective ones of the divide stages further comprise an activation input coupled to receive an activation signal to selectively turn off respective divide stages if the respective divide stages are not used for a desired divide ratio.

24. The clock generation circuit of claim 20 wherein said divider further includes self-correction logic.

25. The clock generation circuit of claim 24 wherein said divider further includes a latch circuit, the latch circuit including:

one or more portions of self-correction logic; and

selection circuitry implementing at least one of the one or more multiplexers.

26. The clock generation circuit of claim 25, wherein:

the selection circuitry is coupled to select respective portions of the self-correction logic based on a selected divide ratio; and

the latch is coupled to outputs of respective portions of the self-correction logic to provide a differential indication of a logic value produced by the selected logic portion.

27. A method comprising:

providing an input clock to a divider, the divider including a sequence of divide stages coupled to selectively provide a plurality of different divide ratios;

clocking each of the divide stages with the input clock; and

selectively feeding back an output of a first divide stage to an input of a second divide stage earlier in the sequence of divide stages.

28. The method of claim 27 further comprising programming the divider to produce a selected divide ratio.

29. The method of claim 27 further comprising selectively turning off one or more divide stages if the one or more divide stages is not used for a desired divide ratio.

30. The method of claim 27 further comprising correcting a duty cycle of an output produced by the divider.

31. The method of claim 30, wherein correcting a duty cycle includes:
generating a first signal having an unbalanced duty cycle;
generating a second signal, wherein the second signal is a delayed version of the first signal; and
logically combining the first signal and the second signal to generate an output signal having a balanced duty cycle.

32. The method of claim 27 further including correcting an abnormal state of one or more divider stages.

33. The method of claim 32 wherein correcting an abnormal state includes:
latching an output of a selected portion of a correction circuit, wherein the portion is selected based, at least in part, on a divide ratio to be achieved.

34. A circuit comprising:
means for providing an input clock to a divider, the divider including means for selectively providing a plurality of different divide ratios;
means for clocking each of the divide stages with the input clock; and
means for selectively feeding back an output of a first divide stage to an input of a second divide stage.

35. The circuit of claim 34 further comprising means for selectively turning off one or more portions of the divider if the one or more portions is not used for a desired divide ratio.

36. The circuit of claim 34 further comprising means for correcting a duty cycle of an output produced by the divider.

37. The circuit of claim 34 further including means for correcting an abnormal state of one or more stages of the divider.

38. The circuit of claim 37 wherein the means for correcting an abnormal state includes means for latching an output of a selected portion of a correction circuit, wherein the portion is selected based, at least in part, on a divide ratio to be achieved.

39. The circuit of claim 34 further comprising means for programming the divider to produce a selected divide ratio.